24.2 A 250mW Full-Rate 10Gb/s Transceiver Core in 90nm CMOS Using a Tri-State Binary PD with 100ps Gated Digital Output

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There is an increasing demand for high-speed serial links as a result of advances in communication networks infrastructure. Standard interfaces such as 10Gb Ethernet are moving into the mass-volume consumer market.

A 90nm CMOS 10Gb/s transceiver core is presented. The transceiver design is targeted for applications in consumer products that require low-power and robustness to jitter. The receiver uses a bang-bang CDR architecture incorporating a tri-state binary PD (BPD) with 100ps-wide up or down pulse output at every rising edge of the data. Both the receive path and the transmit path use the full-rate clock generated by the on-chip VCO, thereby eliminating clock-duty-cycle distortion inherently found in commonly used half-rate architectures [1-3].

The 10Gb/s transceiver-core block diagram is shown in Fig. 24.2.1. The receiver consists of a limiting amplifier (LA), a CDR, and a 1:16 DEMUX. The transmitter comprises a CMU, a retimer, a data output buffer, and a 16:1 MUX. Additionally a BIST block consisting of a parallel 2^7-$1/2^{31}$-1 PRBS pattern generator and checker with 16b loopback function is implemented.

The receiver CDR block diagram is shown in Fig. 24.2.2. The CDR has 2 loops, one is the PFD loop for frequency acquisition, and the other one is the BPD loop for data tracking. A loss-of-lock (LOL) function monitors the difference between the VCO frequency (fvco/N) and the reference frequency (fref). When the bit rate of the received data and the VCO frequency are within ±250ppm, the LOL block automatically switches between the BPD loop and the PFD loop. The BPD, using a similar algorithm as previously reported in [4], consists of the binary-type PD and the associated gating logic block. When the BPD loop is locked, the recovered clock is used by DFF1 in Fig. 24.2.2 to detect the rising data edges, and by DFF0 to retime at the center of the data eye. The following gating logic generates 100ps up or down pulses (equal to one full-rate clock period at 10Gb/s data rate) at every rising data edge. If there are no data transitions, no up or down pulses are generated, thereby minimizing phase drift due to incorrect phase information generated by long runs of consecutive identical digits.

To save power and chip area, the 10GHz LC-VCO directly drives the FFs in the BPD, the divide-by-2, and the buffer for monitoring the recovered 10GHz clock. Potential problems such as frequency pulling and increased jitter are minimized by designing the VCO to swing rail to rail. In addition, the AC-coupling capacitor acts as a voltage divider that effectively reduces the noise coupling back into the VCO. The viability of this technique can be seen in the measurement results, specifically the low recovered clock jitter. According to simulation, this technique reduces the CDR current consumption by about 40%.

In order to improve the speed margin of the CML FF, the topology shown in Fig. 24.2.2 is adopted. Adding the CML inverter to the conventional CML latch reduces the total load capacitance of the latch and improves the speed performance. The FF operation is further improved by the high-amplitude clock signal generated by directly driving from the VCO tank.

The CMU and retiming blocks in the transmitter use a full-rate architecture leading to a decrease in output jitter. This is achieved by retiming the multiplexed data in the 16:1 MUX using the full-rate 10GHz clock [5, 6]. The schematic of the data output buffer including the driver following the 10Gb/s retiming FF is shown in Fig. 24.2.3. The 2 key requirements of this block are: 1) to provide the impedance conversion necessary to drive 50Ω and 2) to provide the wideband routing capability between the output of the retiming block and the input of the output buffer. The transmit side of the interconnection has a common-drain connected NMOS transistor and the receive side has a common-gate connected NMOS transistor. The low impedance presented at both sides of the interconnection enhances the flexibility in layout by reducing bandwidth degradation due to the wiring parasitic capacitance.

The f_t-doubler [7] topology, including the gate-drain capacitance, has ~1/3 of the input capacitance at the expense of half the transconductance compared to the conventional differential buffer. The 4-stage cascaded connection including the f_t-doubler as the final stage, gives a high-bandwidth impedance conversion from the high resistance of the internal CML logic into the low resistance for 50Ω impedance termination and is achieved with low power.

The 10GHz recovered-clock waveform in Fig. 24.2.4 shows an rms jitter of 906fs and a peak-to-peak jitter of 6.7ps. The 5-stage limiting amplifier with an offset-cancellation loop and loss-of-signal (LOS) detection has a gain of 35dB and a 3dB bandwidth of more than 10GHz with an input sensitivity of $5.9mV_{pp\text{-}diff}$ at a BER of 1×10^{-12}. Passive inductive peaking at each stage provides wide bandwidth while maintaining low power consumption. The receiver jitter-tolerance measurement of $0.505UI_{pp}$ at high jitter modulation frequency, over 2MHz, is limited by the test-equipment capability. This wide timing margin is made possible by the large clock signal from the LC tank and the FF used for data regeneration (DFF1 in Fig. 24.2.2).

The transmit eye-diagram, shown in Fig. 24.2.5, has tr/tf of 26.9/25.9ps (20 to 80%) and an amplitude of 568mV. The jitter generation evaluated by Anritsu network-performance tester MP1590B is $5mUI_{rms}$ in loopback mode.

Support for various standard 10Gb/s applications and process-variation tolerance are enabled by the inclusion of automatic initialization blocks, auto coarse frequency control (ACFC), in both the transmitter and receiver. The transmit and receive 10GHz LC-VCOs Vtune-fosc ranges are individually selected by comparing the VCO frequency (fvco/N) and the reference clock frequency and controlling a 4b tuning DAC. The fabricated transceiver core can support applications between 9.9 and 10.8Gb/s. A micrograph of the transceiver is shown in Fig. 24.2.7. The chip occupies $3.26\times2.22mm^2$ including pads. The transmitter consists of the output buffer, retiming block, CMU, and 16:1 MUX and consumes 100mW. The receiver with the limiting amplifier, CDR and 1:16 DEMUX consumes 150mW. A single 1.2V supply is used. All the measurements are evaluated using a 2^{31}-1 PRBS pattern at 10Gb-Ethernet data rate (10.3125Gb/s). The transceiver core performance is summarized in Fig. 24.2.6.

References:

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[7] Carl R. Battjes, "Amplifier Circuit," US Patent 3,633,120.

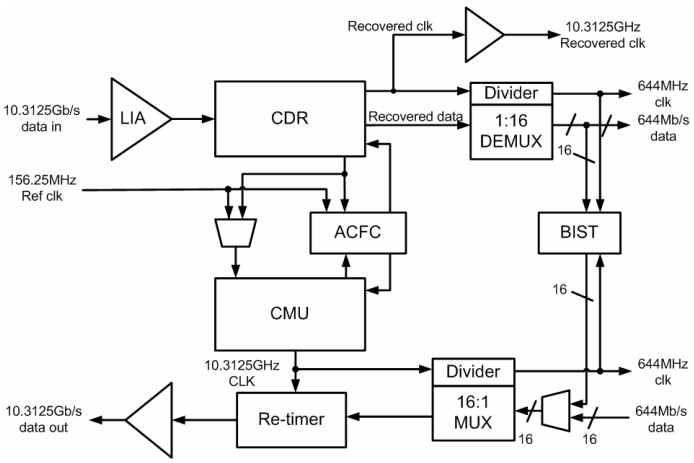

Figure 24.2.1: 10Gb/s transceiver core block diagram.

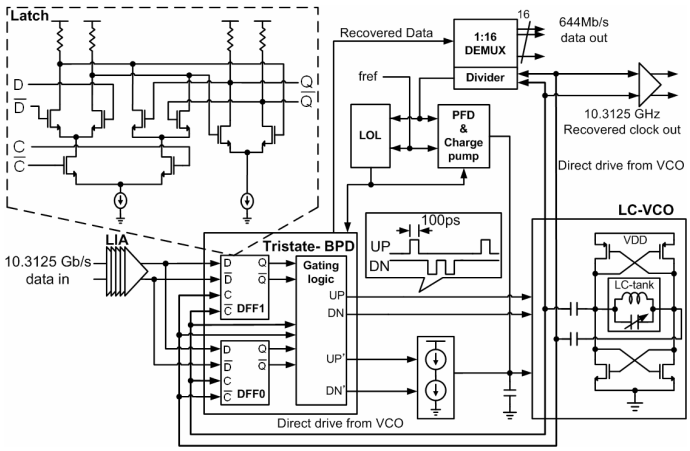

Figure 24.2.2: Full-rate receiver block diagram.

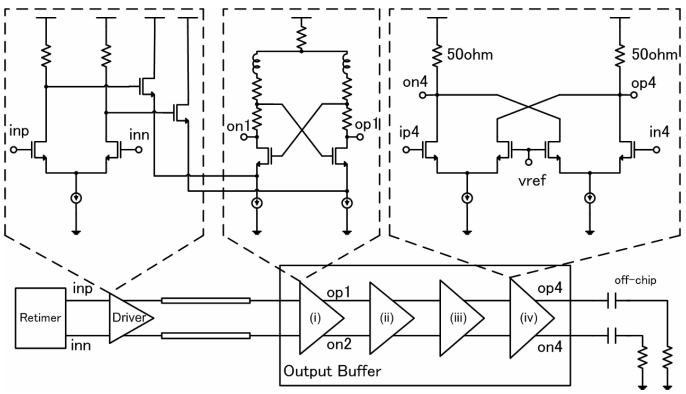

Figure 24.2.3: Output buffer including driver.

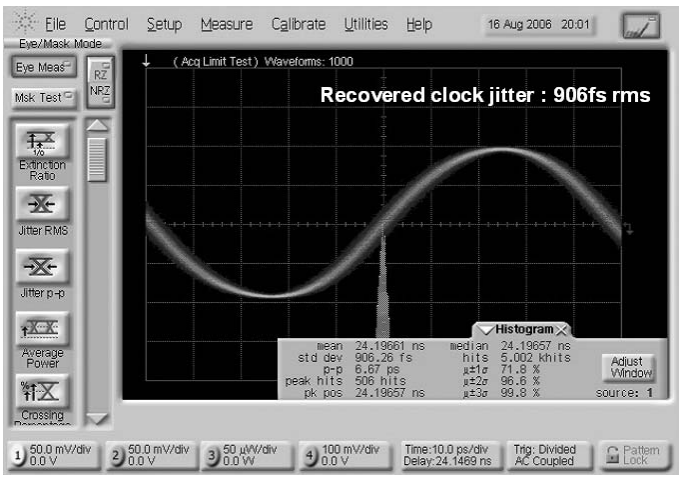

Figure 24.2.4: Recovered-clock jitter performance.

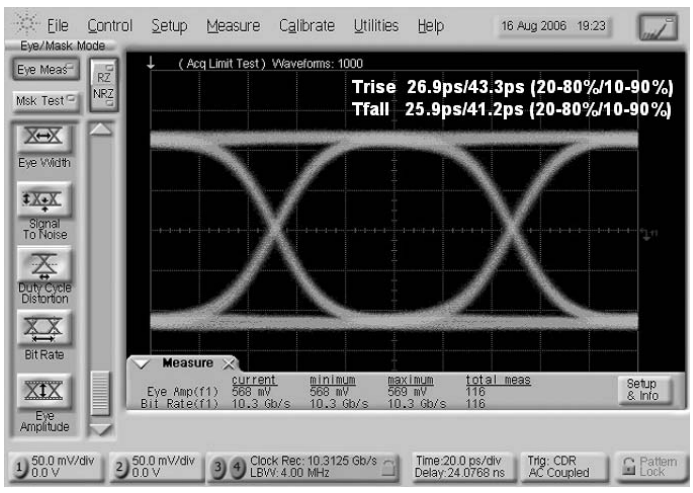

Figure 24.2.5: Transmitter eye diagram.

Process technology		**90nm CMOS**
Input sensitivity		**5.9mV$_{pp\text{-}diff}$**
Recovered clock jitter		**906fs$_{rms}$**
Jitter tolerance		**>0.505UI$_{pp}$**
Jitter generation [filter 50kHz to 80MHz]		**5mUI$_{rms}$**
Power supply		**1.2V**
Power consumption	**Total**	**250mW**
	RX	**150mW**
	TX	**100mW**

Figure 24.2.6: Transceiver core performance summary.

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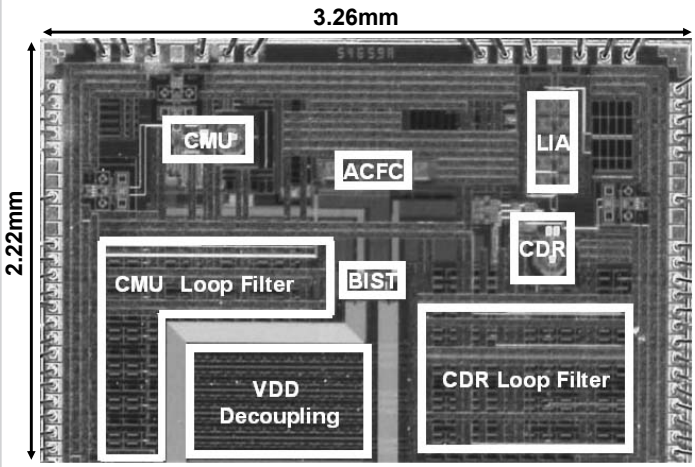

Figure 24.2.7: Micrograph of transceiver core.

